CLAIMS

1. A method for testing an integrated circuit having an embedded device within a configurable logic fabric, comprising:

configuring the configurable logic fabric for a test comprising, forming a scan chain in the configurable logic fabric;

providing scan data from at least a portion of the scan chain to the embedded device; and

performing the test on the embedded device.

2. The method of claim 1 wherein the scan chain comprises a plurality of shift registers connected in series.

3. The method of claim 1 wherein the scan chain comprises a plurality of logic blocks.

4. The method of claim 1 wherein the embedded device is a fixed logic core processor and the method further comprising, using the scan data, placing the fixed logic core processor in a predetermined state.

5. The method of claim 1 further comprising, at least another portion of the scan chain receiving test results from the embedded device.

6. The method of claim 5 further comprising transmitting the test results through the configurable logic fabric to an external tester for evaluation.

7. The method of claim 1 further including transmitting at least one test signal to a multiplexer for delivery to the embedded device.

8. The method of claim 1 further including receiving at least one test output signal from a multiplexer coupled to receive at least one output from the embedded device.

9. The method of claim 1 wherein the embedded device is selected from a group consisting of: a digital signal processor, a microprocessor, a physical layer interface, a link layer interface, a network layer interface, an audio processor, a video graphics processor, a fixed logic circuit, and an applications-specific integrated circuit.

10. A method for testing an integrated circuit (IC), having a configurable logic fabric and a fixed logic circuit, the method comprising:

configuring the IC for test, comprising forming a scan chain having test data;

transferring the test data from the scan chain to a multiplexer, the multiplexer a part of interfacing circuitry, the interfacing circuitry coupling the fixed logic circuit to the configurable logic fabric; and

transferring the test data from the multiplexer to the fixed logic circuit.

11. The method of claim 10 wherein the configuring the IC for test further comprises emulating test functions of an external tester.

12. The method of claim 10 wherein the fixed logic circuit is an embedded core device.

13. The method of claim 12 wherein the embedded core device is a processor.

14. A method for testing a Programmable Logic Device (PLD) having an embedded fixed logic device, comprising:

configuring the PLD for test by forming a scan chain;

sending an output test signal from the embedded fixed

logic device to a multiplexer formed within a gasket; and

sending the output test signal from the multiplexer to the scan chain.

15. The method of claim 14 wherein the PLD is an FPGA.

16. The method of claim 14 wherein the fixed logic device is selected from a group consisting of: a digital signal processor, a microprocessor, a physical layer interface, a link layer interface, a network layer interface, an audio processor, a video graphics processor, a fixed logic circuit, and an applications-specific integrated circuit.

17. A system for testing a fixed logic circuit, comprising:

a programmable logic fabric in an integrated circuit (IC), wherein the fixed logic circuit is embedded in the programmable logic fabric;

interconnecting logic, having a multiplexer, at least partially surrounding the fixed logic circuit, the interconnecting logic coupling the fixed logic circuit to the programmable logic fabric; and

a scan chain formed in the programmable logic fabric for testing the fixed logic circuit via the multiplexer.

18. The system of claim 17 further comprising: a test analyzer formed in the programmable logic fabric for receiving results from the scan chain in order to determine if the fixed logic circuit passed or failed the testing.

19. The system of claim 17 further comprising: an external tester for receiving results from the scan chain in order to determine if the fixed logic circuit passed or failed the testing.

20. The system of claim 17 wherein the scan chain is reconfigured to test the interconnecting logic.

21. The system of claim 17 wherein the fixed logic circuit is selected from a group consisting of: a digital signal processor, a microprocessor, a physical layer interface, a link layer interface, a network layer interface, an audio processor, a video graphics processor, a fixed logic circuit, and an applications-specific integrated circuit.

22. The system of claim 17 wherein the programmable logic fabric is part of a field programmable gate array.

23. The system of claim 17 further comprising:

test results produced from the fixed logic circuit; and

a comparator formed in the programmable logic fabric to compare the test results to expected output values received from a memory.

24. The system of claim 17 wherein the interconnecting logic further comprises: on Chip Memory controller modules for interfacing the fixed logic circuit with memory in the programmable logic fabric, a multiplexer array having the multiplexer, and a controller coupled to the fixed logic circuit.

25. The system of claim 17 wherein the scan chain comprises a latch shift register.

26. The system of claim 25 wherein the latch shift register comprises:

a first circuit having a multiplexer coupled to a first latch and an OR gate multiplexer coupled to the first latch; and

a second circuit having a second latch coupled to the first circuit.

27. A method for testing an integrated circuit (IC),

having a configurable logic fabric with an embedded fixed logic circuit, wherein the embedded fixed logic circuit has a surrounding interface logic for interfacing the embedded fixed logic circuit with the configurable logic fabric, the method comprising:

configuring the IC for test, comprising forming a scan chain having first test data;

transferring the first test data from the scan chain to a first multiplexer; and

transferring the first data from the first multiplexer to a first portion of the interface logic for testing the first portion of the interface logic.

28. The method of claim 27 further comprising:

transferring second test data from the scan chain to a second multiplexer; and

transferring the second test data from the second multiplexer to the embedded fixed logic circuit for testing the embedded fixed logic circuit.

29. The method of claim 28 further comprising:

sending third test data from the scan chain to a second portion of the interface logic; and

sending first results of the third test data to the scan chain, wherein the second multiplexer prevents the first results being transferred to the embedded fixed logic circuit.

30. The method of claim 29 further comprising:

sending second results from the embedded fixed logic circuit to the scan chain, wherein the first multiplexer prevents the second results being transferred to the first portion of the interface logic.